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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,539	04/15/2002	Anand S. Murthy	42390.P6624PCT	6105
7590	12/09/2003			
Blakely Sokoloff Taylor & Zafman 12400 Wilshire Blvd Seventh Floor Los Angeles, CA 90025			EXAMINER KEBEDE, BROOK	
			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 12/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/831,539	MURTHY ET AL.
	Examiner Brook Kebede	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.

- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.

- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.

- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 03 November 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 11 and 13-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 11 and 13-21 is/are allowed.

6) Claim(s) 22-30 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) The translation of the foreign language provisional application has been received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s) _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 3, 2003 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 22-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (JP/63076481).

Re claim 22, Horiuchi et al. disclose a method of making a transistor, comprising: forming a dielectric (3) on a first surface of a wafer (1); forming a conductive layer (4) overlying the dielectric (3); patterning the conductive layer (4) to form a gate electrode (4) and patterning the dielectric (3) so as to form a gate dielectric (see Fig. 3B); forming recesses (not labeled) adjacent and partially subjacent the gate structure(3 4 5 18); and in a continuous operation, back filling the recesses with doped crystalline material (9 10 91 101), wherein back filling comprises forming crystalline material of at least a first conductivity type within a portion of the recess partially adjacent the gate dielectric and gate electrode (see Figs. 3B-3D).

Re claim 23, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 3B-3D).

Re claim 24, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein back filling further comprises forming crystalline material of a second conductivity type with the portion of the recess partially subjacent the gate dielectric and the gate electrode (see Figs. 3B-3D).

Re claim 25, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 3B-3D).

Re claim 26, as applied to claim 25 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein back filling comprises a selective deposition (see Figs. 3B-3D).

Re claim 27, Horiuchi et al. disclose a method of fabricating a FET, comprising: forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type; forming first spacers along the sidewalls of the gate electrode; forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface; substantially filling the recess with a first layer of doped crystalline material, the first layer having a second conductivity type (see Figs. 3B-3D).

Re claim 28, as applied to claim 27 above, Horiuchi et al. disclose all the claimed limitations including the limitation further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate (see Figs. 3B-3D).

Re claim 29, as applied to claim 27 above, Horiuchi et al. disclose all the claimed limitations including the limitation forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess (see Figs. 3B-3D).

Re claim 30, as applied to claim 29 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power in the range of approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium (see Figs. 3B-3D).

Allowable Subject Matter

4. Claims 11 and 13-21 are allowed over prior art of record.
5. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach “selectively forming a layer of a second material having a second

conductivity type over, and within the portion that underlies the gate electrode," as recited in claim 11.

Claims 13-21 are also allowed as being dependent of the allowed independent base claim.

Response to Arguments

6. The following is a statement of reasons for the indication of allowable
7. Applicant's arguments filed November 3, 2003 have been fully considered but they are not persuasive.

With respect to claim 22, applicants argued that "Horiuchi does not teach these limitations, and in contrast teaches backfilling a region that is not subjacent or underlying the gate electrode or gate dielectric with a doped material, as illustrated in Horiuchi figure 3D. In figure 3D Horiuchi illustrates the backfilled drain regions 9, 91,10, and 101 containing doped material. The regions 72 of Horiuchi's figure 3D that do underlie the gate electrode are insulator regions and not a doped crystalline material ..." In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particular, as stated above. The Examiner respectfully submits that Horiuchi et al. disclose all the claimed limitation as applied herein above. As shown Fig. 3D both layers 9 91 and 10 101 uses as source/drain electrode are arsenic (As) doped amorphous silicon layer which crystallized during annealing and also Fig. 3D clearly teaches the limitation of "back filling the recesses, including the portion of the recesses that partially subjacent the gate structure, with doped crystalline material." In addition see the specification in Pages 407-408.

Furthermore, applicants' argument with respect to claim 27 has no merit because Horiuchi et al. also disclose the limitation "substantially filling the recess that extends laterally

through the substrate so as to underlie a portion of the gate electrode with a first layer doped crystalline material (see Fig. 3D).

Therefore, the rejection under 35 U.S.C. 102 is deemed proper.

Conclusion

8. THIS ACTION IS MADE NON-FINAL.

Correspondence

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511.

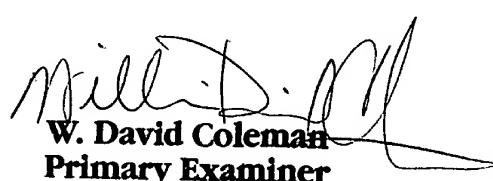
After February 4, 2004, the Examiner should be contacted at (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
December 6, 2003


W. David Coleman
Primary Examiner